IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	)	
Michael Ray Timperman, et al.	)	Group: 2661
Serial No.: 09/957,008	)	
Filed: September 20, 2001	)	
Title: DATA PACKET COMMUNICATION DEVICE	)	Examiner: J. Park

DECLARATION UNDER 37 C.F.R. §1.131(a)

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Michael Ray Timperman and Jason Eric Waldeck, the Applicants in the above-identified patent application, declare as follows:

1. That sometime prior to July 9, 2001, we conceived of a Data Packet Communication Device (hereinafter, the DEVICE).

2. That according to one aspect of the DEVICE, a method of processing data packets included receiving a plurality of the data packets at a selected node; extracting pertinent information from the data packets, the pertinent information being pertinent to said selected node; and generating a plurality of response data packets based on the pertinent information, wherein said extracting and generating steps are performed without use of a microprocessor. The method included transmitting a signal indicating that the response data packets should be sent.

3. That according to another aspect of the DEVICE, a data packet communication system included a peripheral device; and a filter device connected to said peripheral device, said filter device being configured to receive a plurality of data packets and identify pertinent information

in said data packets, said pertinent information being pertinent to said peripheral device. The system included a packet generator connected to said peripheral device and said filter device, said packet generator being configured to generate a plurality of response data packets based on said pertinent information. The packet generator is configured to transmit said response data packets. The filter device is configured to transmit a signal indicating that said response data packets should be generated. The packet generator is configured to transmit said response data packets to a packetized data network. The system included a protocol state machine configured for receiving the signal from said filter device and issuing a request to said packet generator to transmit said response data packets.

4. That according to another aspect of the DEVICE, a data packet communication device included a filter device configured to receive a plurality of data packets and identify pertinent information in said data packets; and a packet generator configured to generate a plurality of response data packets based on said pertinent information. The filter device is configured to transmit a signal indicating that said response data packets should be generated. A protocol state machine is configured for receiving the signal from said filter device and issuing a request to said packet generator to transmit said response data packets.

5. We, the Applicants, prepared an Invention Disclosure (see **Exhibit A**) entitled, "PACKET COMMUNICATION HARDWARE," which was signed and dated prior to July 9, 2001, although the dates have been redacted from the copy of the Invention Disclosure at Exhibit A.

6. A patent application directed to the Invention Disclosure was filed in the U.S. Patent Office on September 20, 2001, and was assigned U.S. Patent Application Serial No. 09/957,008.

The declarants further state that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Michael Ray Timperman — Date: Oct. 12. 2005

Jason Eric Waldeck — Date: Oct. 12 2005

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LEXMARK	**Invention Disclosure** Status: Final	Disclosure Number: 2001-0134.00 Date Submitted: [redacted] Docket Number:

Title of the Invention

Packet Communication Hardware

Inventor(s)	Serial#	Division	Department	Building	Location	Phone
Jason Waldeck	0604218	BPD	501C17L	[redacted]	Lexington	[redacted]
Mike Timperman	0285803	BPD	501C18L		Lexington	

Additional Inventors:

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Signature of Inventor	Date	Signature of Inventor	Date
Jason Waldeck	[redacted]		

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	[redacted]		[redacted]

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Summary of the Invention
(Provide a brief summary of the Invention.)

This invention provides a means for network communication using specialized hardware that eliminates the need for a microprocessor in the system. The result is a minimal-cost packet processing node.

Product Code Name: [redacted]
Additional Product Code Names:
Scheduled Announce Date: [redacted]
This disclosure will not be processed by the IP Law Department until the above product information is completed.

Are there additional hard-copy materials to be included? No

Evaluator: Tom Knight	**Attorney:** Jacki Daspit

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PacketHardware.doc

Background of the Invention

(Describe the technical setting of the invention and cite any known prior art.)

The invention relates to the processing of information in a packetized communication system. In particular, the invention concerns a hardware apparatus that extracts only pertinent information from received packets and can generate response packets based on the same information. This processing is done in real time and without the use of an additional data processing system that might consist of a microprocessor or storage memory.

In many communication systems, any transmission from one node is sent to a plurality of connected nodes. In such broadcast systems, the information may only be relevant to a single receiver, but all nodes must process the transmission to determine its intent. Data on such networks are usually broken into pieces known as packets. A packet consists of consecutive bytes that may be marked by leading and/or trailing delimiters. Protocols by which nodes communicate usually divide a packet into the protocol-relevant information (the header) and the data relevant to the receiving node (payload).

In many environments the protocols are "layered" so that the payload area of a lower protocol contains a packet of the next higher layer protocol. Most communication environments require that addressing information be contained at fixed locations (in the first few bytes) of the lowest layer protocol header so that hardware can help discard unwanted packets by simple filtering.

There are many examples of commercially available network devices that perform such filtering. Practically all Ethernet media access controllers (MAC's), for instance, provide for filtering based on an exact match of the first six bytes of a packet header to a programmed value (the network address). This greatly reduces the load of the general-purpose central processing unit (CPU). However, many network frames that are addressed to the node either distinctly or by a shared address are still not relevant to a particular node. The receiving equipment may be required to look at an entire packet to determine its relevance. Additional cost is inherent in networked systems because memory is required to store the entire packet while the processing elements perform the analysis.

There are many prior patents relating to the field of packet filtering. Most of these are a result of the very competitive commercial network switch and router market. Routers must sort received frames into subsets based on different byte fields within a packet. To achieve high throughput, many inventions use specialized hardware to perform this sorting (see US5608662, US5761424, US5574910, or US6041058 for example). These inventions make the assumption that a CPU is present and only assist the microprocessor in performing its task.

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Detailed Description of the Invention

(Provide a thorough description of the invention and how it works.)

The present invention improves upon the prior art by eliminating the need for a microprocessor to participate in the network packet processing. Packet filter hardware not only identifies packets relevant to the receiving node, but also extracts any pertinent information contained in the data stream. Signals are created by the filter hardware to indicate that a response packet should be generated using the extracted information. The packet filter hardware can be replicated and used in parallel to provide different protocols within the same network node.

FIGURE I is a schematic that illustrates the overall system architecture, which connects the hardware filter and packet generator to a packet data network and an interface to the payload data consumer. An optional protocol state machine may be necessary to convert filter indications into transmit requests to the packet generator. The network may be any of the common serial network architectures (such as Ethernet or Token Ring) or generally any packetized data stream. The data consumer could be any reasonable system that utilizes information, i.e., a computer, printer, set-top box, or other peripheral. The details of the interface to such a device varies, but typically consists of a FIFO memory or data buffer.

FIGURE II illustrates the format of a possible network packet. Only fields of interest to the receiving node are important, with other packet bytes being treated as "don't care" information that can be ignored. Bytes of interest include the payload data as well as header data that might identify the packet type, the intended receiver, checksum information, sequencing information, and so forth.

FIGURE III shows the filter hardware in detail. Its primary blocks are the offset counter, pattern generator, mask generator, multiplexer, maskable comparator, event decoder, and the signaling logic. All of the blocks are simple to construct by someone skilled in the art, and therefore limited schematics of each block are presented here. The incoming packet data stream is assumed to be a stream of words (of fixed bit-width W) with start of packet (SOP) and end of packet (EOP) indicators that are synchronous to a common receive clock. This is a common interface for MAC hardware. The outputs of the block consist of the extracted payload data stream, protocol parameters, and indicators of a successfully accepted packet.

The offset counter consists of an N-bit counter that tracks the number of words from the start of a packet. The counter must be wide enough to accommodate a maximum-length packet for the particular network medium. The offset counter is cleared upon receiving the SOP indication and increments by one with each packet word received.

The pattern generator is a special case of an N to M decoder. Given an input value of width N, the pattern generator outputs a predetermined corresponding word of width M. The decoder is designed so that given the input packet offset, its output is the corresponding word required for packet acceptance.

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The mask generator is similar to the pattern generator. It decodes the offset counter and produces a bit-mask. The mask indicates which bits within the word are compared. An additional set of outputs is routed to the multiplexer. These outputs determine whether the multiplexer should pass the output of the pattern generator or one of the external comparison values to the comparator block. The external comparison values are specific to the receiving node (such as its network address) or are states within the protocol. For protocols where it is only necessary to examine entire words, only the multiplexer control outputs are necessary.

The maskable comparator indicates whether the bits in the received packet word unmasked by the bit generator are equal to the corresponding bits in the output of the multiplexer. A logical '0' indicates that all unmasked bits match. If the word is a don't care (all bits masked), the output is also a '0'.

The event decoder is a simple decoder that indicates when header information needs to be stored into memory elements (flip-flops). This allows the protocol state machine or transmitter to use the information when updating its state or transmitting a response. The event decoder is also used to generate a Payload Start (PS) signal to indicate where in the packet payload data should be extracted.

The signaling logic block is used to generate indicators to outside entities. Its details are shown in FIGURE IV. A signal, RELEVANT, is generated with an R-S flip-flop. The Start of Packet signal is connected to the 'S' input, with the 'R' input connected to the output of the maskable comparator. Thus, RELEVANT goes high at the start of a packet and remains high until the comparator finds a problem with the packet. The RELEVANT signal is logically AND'ed with the End of Packet signal to create a PACKET_GOOD signal for use outside the filter block. The PAYLOAD_VALID signal is also generated by an R-S flip-flop. The Payload Start signal is AND'ed with the RELEVANT signal and connected to the 'S' input. The End of Packet signal is connected to the 'R' input. This creates a signal that is active for the entire payload of packets whose header matches the acceptable criteria.

The packet filter operates as follows. When the Start of Packet indicator is given, the offset counter is cleared and the RELEVANT signal is set active. Packet data starts entering the filter, with the counter incrementing with each word. At each word, the mask generator determines whether any part of the word is necessary for comparison. It also determines which value should be used for the comparison (the output of the pattern generator or one of the external comparison values). Note that the output of the pattern generator is a "don't care" condition whenever a comparison is not performed. The multiplexer steers the appropriate compare word to the comparator block. The comparator block indicates if a necessary match is missing. If it is so indicated, the RELEVANT signal will drop inactive and processing, though continuing on, is therefore ignored for the remainder of the packet. If the header is successfully processed (the Payload Start signal is generated), then the EXTRACTED_VALID signal activates and the packet payload data is passed to the peripheral for consumption. This continues until the End of Packet signal is indicated, which causes the EXTRACTED_VALID signal to deactivate and the PACKET_GOOD signal to be pulsed.

Meanwhile, the latch decoder extracts header data by activating the enable inputs of storage flip-flops attached to the data stream. When the PACKET_GOOD signal is pulsed, the protocol state machine can determine if a response is necessary. If such a response is called for, the extracted header information is then available to the packet generator as header input data for transmission.

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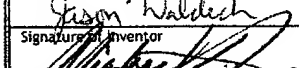
Signature of Inventor 	Date [redacted]	Signature of Inventor	Date
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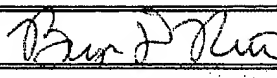
Signature of Witness 	D[redacted]	Signature of Witness 	[redacted]

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There are several variations of the packet filter block that might be needed for difficult protocols. The comparator could include more ALU-like functions (less than, greater than, etc.) than merely the 'equals' operation. The pattern, mask, and latch generators could be replicated and connected in parallel to identify various types of packets.

Multiple filter blocks could be used in parallel to detect different protocols, or might be cascaded serially to allow for the stripping of the individual protocol layers, as needed.

FIGURE V illustrates the components of the associated packet generator. It uses the same building blocks as those found in the packet filter. The packet generator consists of an offset counter, a pattern generator, a multiplexer, an event decoder, and a mask generator.

The offset counter, pattern generator, event decoder, and multiplexer perform the same functions as those used in the packet filter. The pattern generator may or may not have the exact same patterns as the receive side—it is protocol dependent.

The mask generator is only used to create the multiplexer steering controls. The masks need not be generated since no comparisons are performed on the transmit side.

The packet generator operates exactly as the logic used to create the comparison word in the packet filter. When a packet is to be sent, the offset counter is cleared and the generators decode the offset into a transmission word. This word is sent to the Media Access Controller for transmission. When the MAC requires the next word, the offset counter is incremented and the process continues until all words of a packet have been sent. The event decoder creates the necessary framing signals SOP and EOP.

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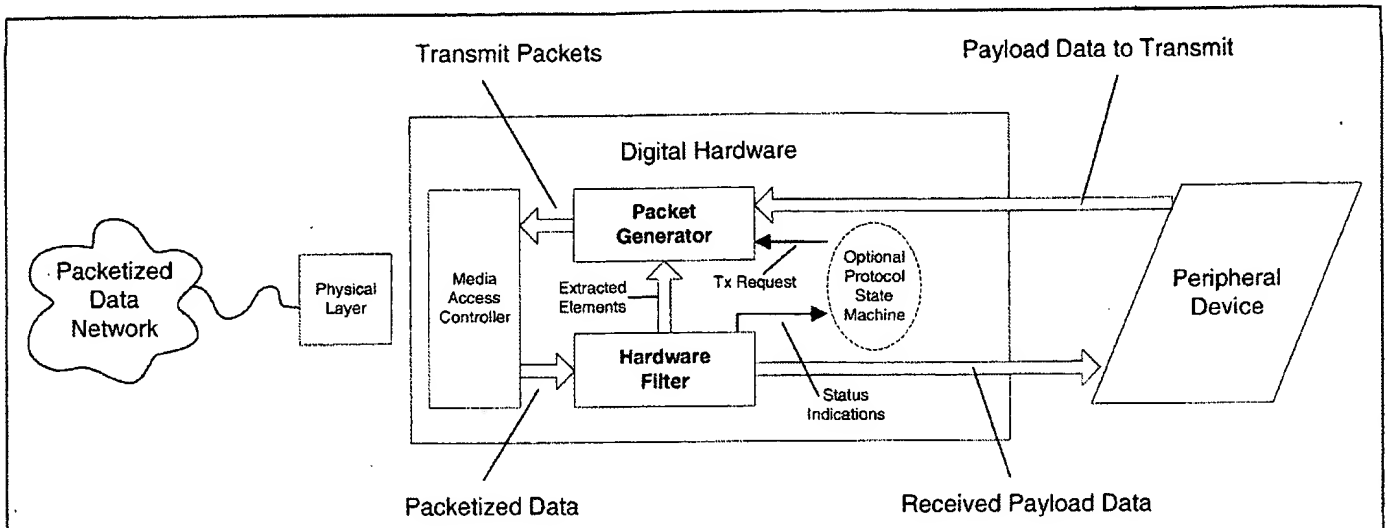

FIGURE I

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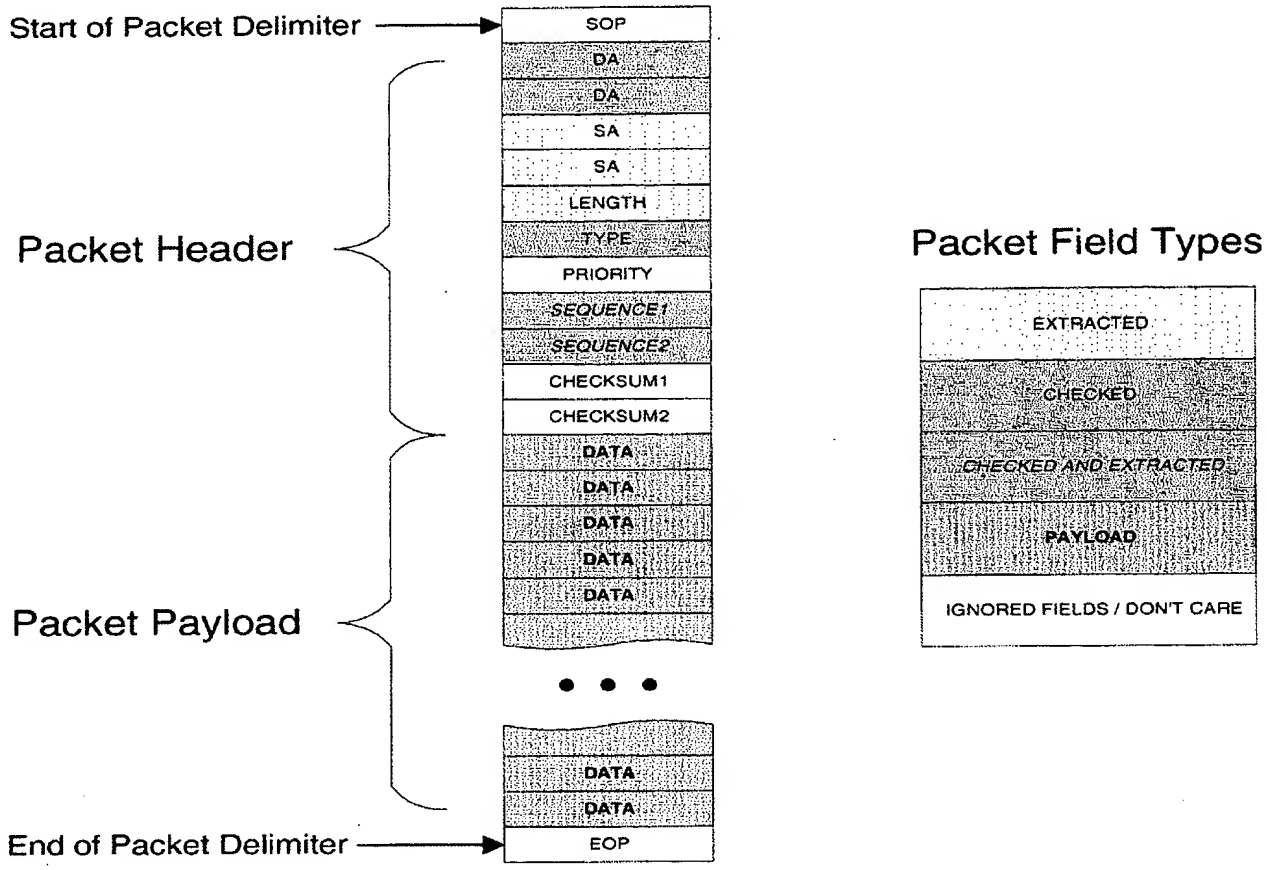

FIGURE II

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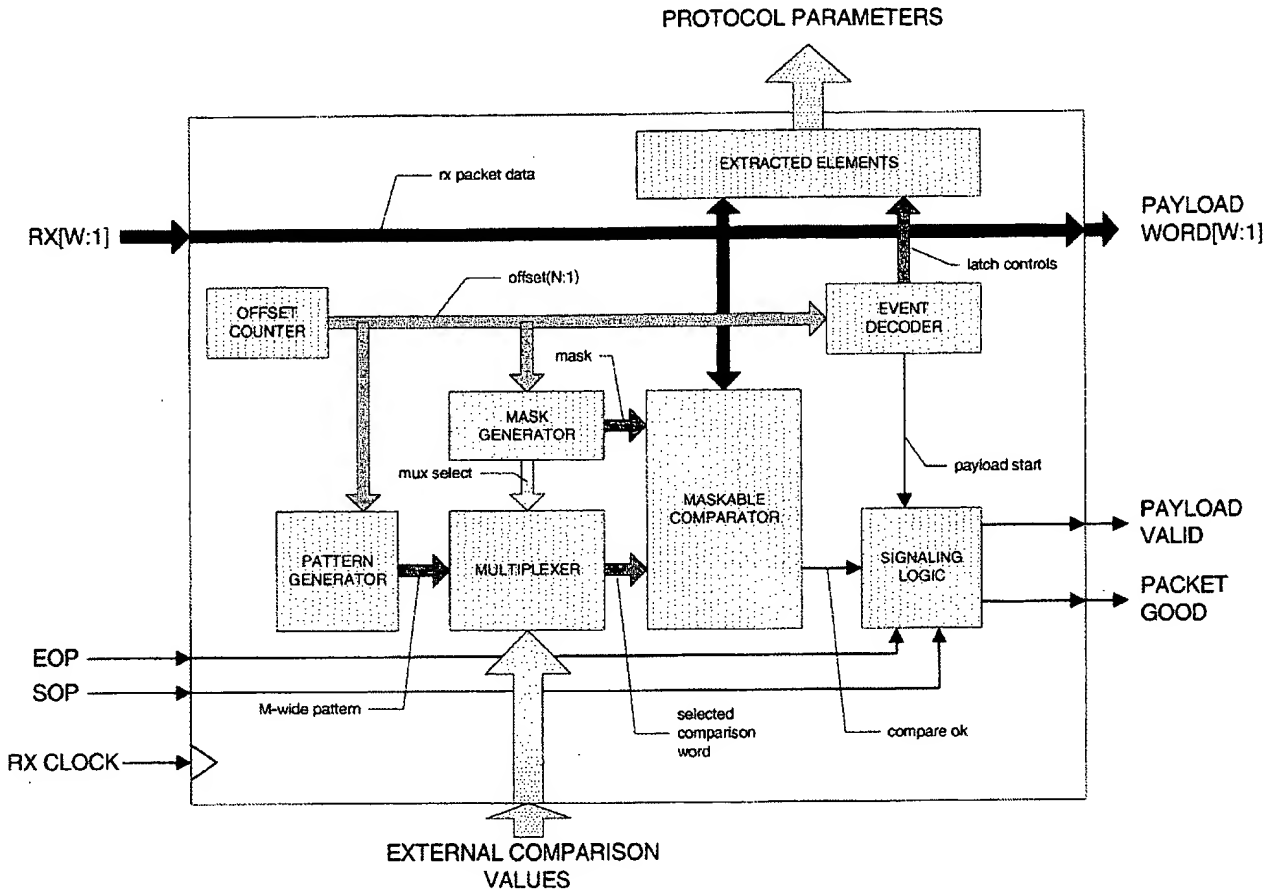

FIGURE III

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Signature of Inventor		Signature of Inventor	Date
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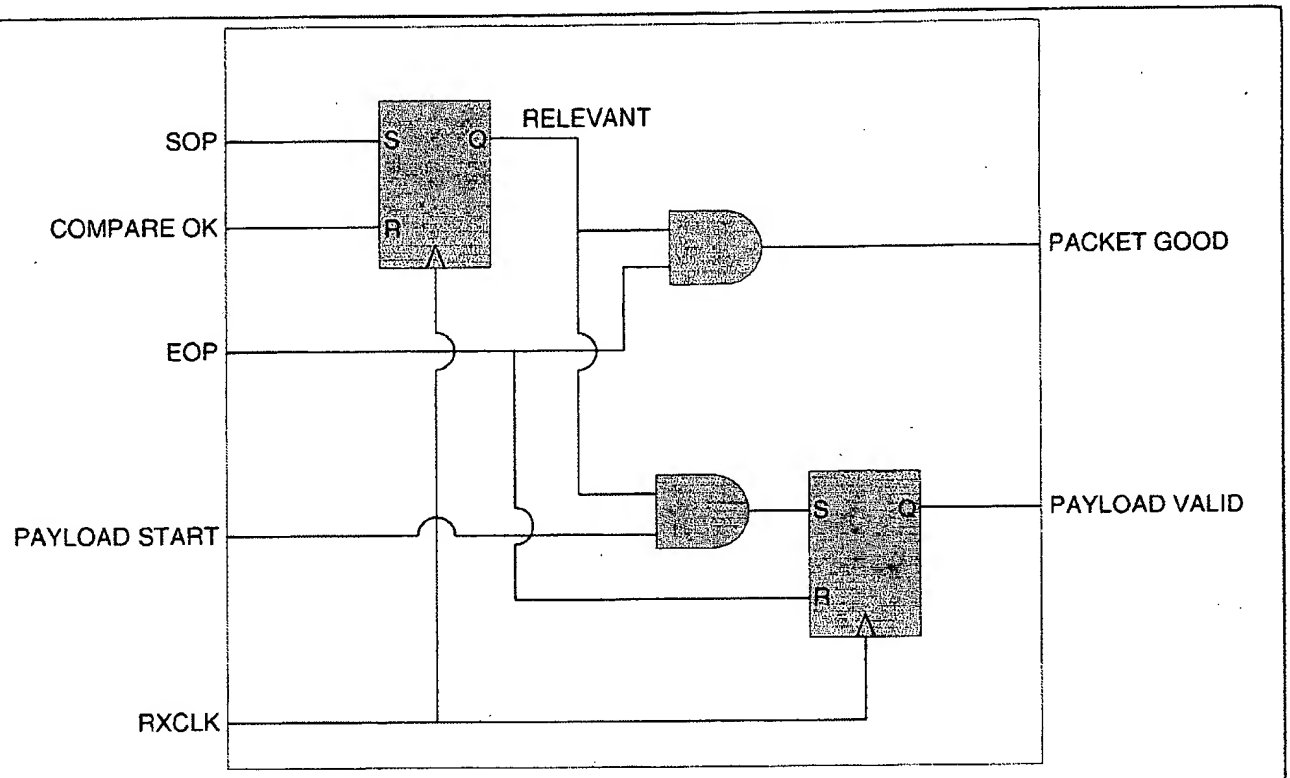

FIGURE IV

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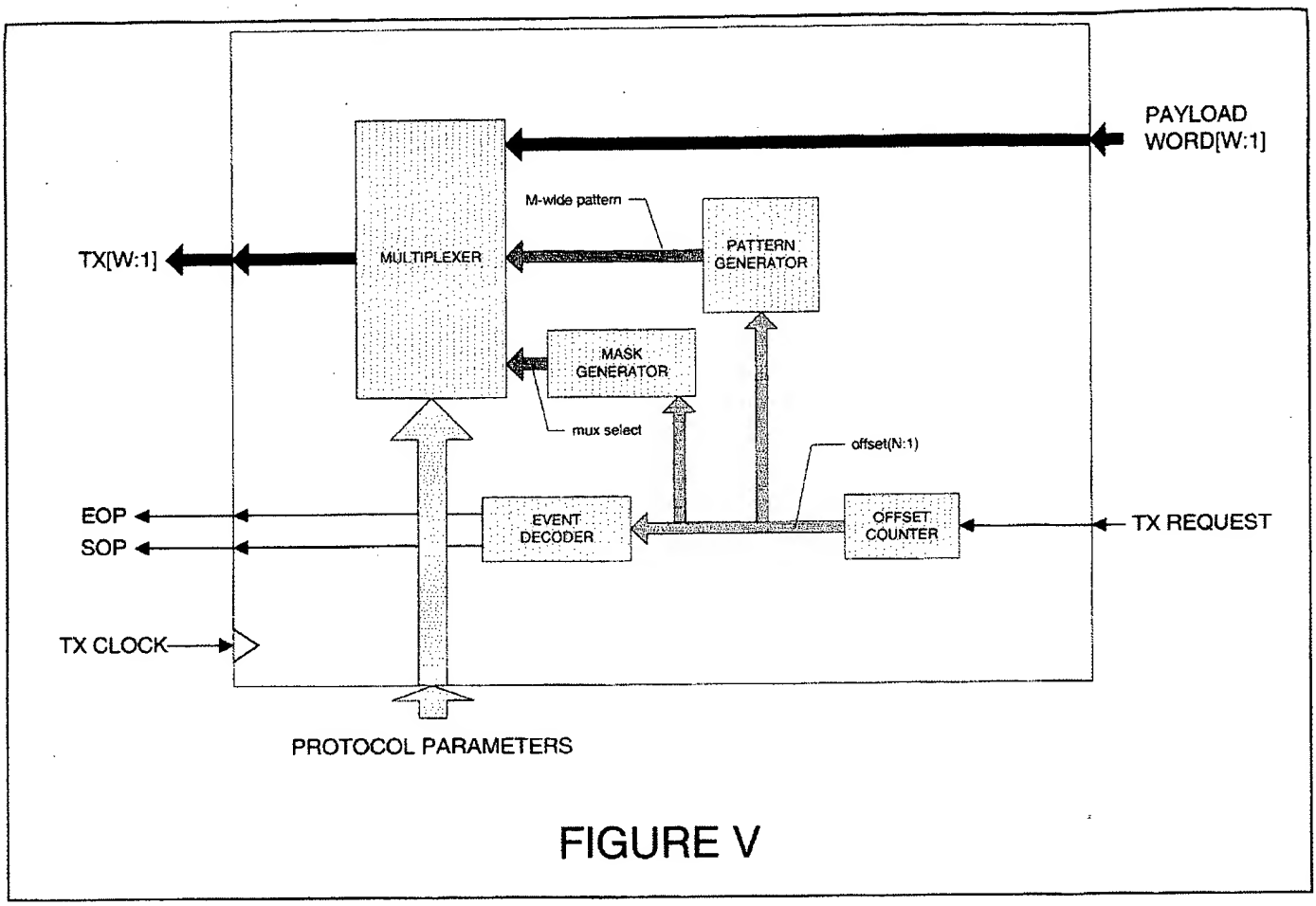

FIGURE V

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